AMENDMENTS TO THE CLAIMS

This listing of the claims, in which new claims 2-33 are being added, will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (original) A method of maintaining a predetermined phase relationship between a periodic output signal and a periodic input signal, said method comprising:

counting signals that each indicate a phase difference outside said phase relationship between said output signal and said input signal; and

shifting the phase of said output signal to reestablish said phase relationship in response to said counting signals reaching a count threshold, said count threshold greater than one.

2. (new) The method of claim 1 wherein:

said counting comprises counting signals indicating a lagging phase difference; and

said shifting comprises shifting the phase of said output signal to reestablish said phase relationship in response to said counting signals reaching a lagging phase count threshold, said count threshold greater than one.

3. (new) The method of claim 1 wherein:

said counting comprises counting signals indicating a leading phase difference; and

said shifting comprises shifting the phase of said output signal to reestablish said phase relationship in response to said counting signals reaching a leading phase count threshold, said count threshold greater than one.

4. (new) The method of claim 1 wherein said counting comprises:

counting signals that indicate a lagging phase difference outside said phase relationship between said output signal and said input signal;

counting signals that indicate a leading phase difference outside said phase relationship between said output signal and said input signal; and

taking the difference between said counted signals indicating a lagging phase difference and said counted signals indicating a leading phase difference.

5. (new) The method of claim 4 wherein said shifting comprises shifting the phase of said output signal to reestablish said phase relationship in response to said difference reaching said count threshold, said count threshold greater than one.

6. (new) Apparatus comprising:

a phase detector having a first input operative to receive a periodic reference signal, a second input, and an output, said detector operative to detect phase differences between respective signals received at said first and second inputs;

a thermometer register having an input and an output, said register input coupled to said phase detector output, said register providing an output signal in response to all bits of said register having a same logical binary value; and

a variable-delay buffer having a first input operative to receive said reference signal, a second input coupled to said register output, a plurality of delay elements, and an output operative to provide an output signal,

said output signal coupled to said second input of said phase detector, said buffer operative to select a delay with respect to said reference signal at which to output said output signal in response to said register output signal.

7. (new) The apparatus of claim 6 wherein said apparatus comprises a delay lock loop.

8. (new) The apparatus of claim 6 wherein said apparatus comprises a memory device.

9. (new) The apparatus of claim 6 wherein said apparatus comprises a dynamic random access memory.

10. (new) The apparatus of claim 6 wherein said apparatus comprises a synchronous dynamic random access memory.

11. (new) The apparatus of claim 6 wherein said phase detector comprises a flip-flop clocked by said reference signal, said flip-flop coupled to receive said buffer output signal and providing an output signal indicative of whether said buffer output signal is leading or lagging said reference signal.

12. (new) The apparatus of claim 6 wherein said thermometer register comprises a shift register.

13. (new) The apparatus of claim 6 wherein:

the most significant bits of said thermometer register are initialized to a same logical binary value, said most significant bits representing half of all bits in said thermometer register; and

the least significant bits of said thermometer register are initialized to the other logical binary value, said least significant bits representing the other half of all bits in said thermometer register.

14. (new) The apparatus of claim 13 wherein:

said most significant bits are initialized to logical ones; and

said least significant bits are initialized to logical zeros.

15. (new) The apparatus of claim 6 wherein:

said thermometer register is shifted in a first direction in response to a phase detector output signal indicating a lagging buffer output signal; and

said thermometer register is shifted in a second direction opposite said first direction in response to a phase detector output signal indicating a leading buffer output signal.

16. (new) The apparatus of claim 15 wherein:

said shift in a first direction comprises shifting in a bit having a logical binary value; and

said shift in a second direction comprises shifting in a bit having the other logical binary value.

17. (new) The apparatus of claim 6 wherein said register output signal comprises:

a first register output signal indicating that said delay should be increased; and

a second register output signal indicating that said delay should be decreased.

18. (new) The apparatus of claim 6 wherein said register output signal comprises:

a first register output signal that is output in response to said thermometer register having all logical ones; and

a second register output signal that is output in response to said thermometer register having all logical zeros.

19. (new) Apparatus comprising:

a phase detector having two outputs, a first input operative to receive a first periodic signal, and a second input operative to receive a second periodic signal, said detector generating a first signal at said first output in response to detecting said second periodic signal with a leading phase difference outside a predetermined phase relationship with said first periodic signal and generating a second signal at said second output in response to detecting said second periodic signal with a lagging phase difference outside said phase relationship;

means for determining the number of said generated first and second signals, said means generating a third signal in response to said first signal being greater than said second signal by a first predetermined number and generating a fourth signal in response to said second signal being greater than said first signal by a second predetermined number; and

a variable-delay buffer coupled to said means, said buffer adjusting the phase of said second periodic signal in response to receiving one of said third and fourth signals.

20. (new) The apparatus of claim 19 wherein said apparatus comprises a delay lock loop.

21. (new) The apparatus of claim 19 wherein said apparatus comprises a memory device.

22. (new) The apparatus of claim 19 wherein said apparatus comprises a dynamic random access memory.

23. (new) The apparatus of claim 19 wherein said apparatus comprises a synchronous dynamic random access memory.

24. (new) The apparatus of claim 19 wherein:

said third signal causes said buffer to adjust said phase by increasing a delay between said first and second periodic signals; and

said fourth signal causes said buffer to adjust said phase by decreasing a delay between said first and second periodic signals.

25. (new) The apparatus of claim 19 wherein said phase relationship comprises a zero phase difference between said first and second periodic signals.

26. (new) A memory device comprising:

a phase detector operative to detect the phase difference between two signals, said phase detector having an output;

a low pass filter having an input coupled to said phase detector output, said filter having an output and operative to output a first signal in response to receiving from said phase detector a first predetermined number of a first type of signal and operative to output a second signal in response to receiving from said phase detector a second predetermined number of a second type of signal, said first and second predetermined numbers each greater than one; and

a delay buffer having an input coupled to said filter output and having a second input operative to receive one of said two signals, said delay buffer operative to output the other of said two signals and operative to increase or decrease a phase difference between said two signals in response to and in accordance with receipt of either said first or said second signal from said filter output.

27. (new) The memory device of claim 26 wherein said memory device comprises a dynamic random access memory.

28. (new) The memory device of claim 26 wherein said memory device comprises a synchronous dynamic random access memory.

29. (new) The memory device of claim 26 wherein:

said first predetermined number is a predetermined positive net number of said first type signals greater than said second type signals; and

said second predetermined number is a predetermined positive net number of said second type signals greater than said first type signals.

30. (new) The memory device of claim 26 wherein said first type signal indicates a lagging phase difference and said second type signal indicates a leading phase difference.

31. (new) The memory device of claim 26 wherein said first signal output from said low pass filter is a logical one signal and said second signal output from said low pass filter is a logical zero signal.

32. (new) The memory device of claim 26 wherein said low pass filter output comprises two signal leads, said first signal output on one of said two leads and said second signal output on the other of said two leads.

33. (new) A memory device comprising:

means for counting signals that each indicate a phase difference outside a predetermined phase relationship between a periodic output signal and a periodic input signal; and

means for shifting the phase of said output signal to reestablish said phase relationship in response to said counting signals reaching a count threshold, said count threshold greater than one.